10/625,917 C 07-C

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

In re application of: Shahram Mostafazadeh

Attorney Docket No.: NSC1P194D1/P04836D1

Patent: 6,975,038 B1

Issued: December 13, 2005

Title: CHIP SCALE PIN ARRAY

CERTIFICATE OF MAILING
I hereby certify that this correspondence is being deposited with the U.S. Postal Service with sufficient postage as first-class mail on April 28, 2006 in an envelope addressed to the Commissioner for Patents, P.O. Box 1450 Alexandria, VA 22313-1450.

Signed: _____
Aurelia M. Sanchez

REQUEST FOR CERTIFICATE OF CORRECTION OF OFFICE MISTAKE (35 U.S.C. §254, 37 CFR §1.322)

Commissioner for Patents
P.O. Box 1450
Alexandria, VA 22313-1450
Attn: Certificate of Correction

Dear Sir:

Attached is Form PTO-1050 (Certificate of Correction) at least one copy of which is suitable for printing. The errors together with the exact page and line number where the errors are shown correctly in the application file are as follows:

CLAIMS:

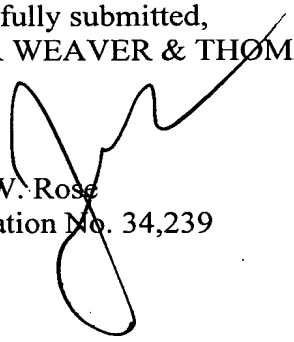
1. In line 7 of claim 13 (column 9, line 2) change "fit die" to --first die--. This appears correctly in Amendment C as filed on April 25, 2005, on page 3, paragraph 6, line 4.

2. In line 13 of claim 19 (column 10, line 18) change "act to" to --acting to--. This appears correctly in Amendment C as filed on April 25, 2005, on page 4, paragraph 6, line 9.

Patentee hereby requests expedited issuance of the Certificate of Correction because the error lies with the Office and because the error is clearly disclosed in the records of the Office. As required for expedited issuance, enclosed is documentation that unequivocally supports the patentee's assertion without needing reference to the patent file wrapper.

It is noted that the above-identified errors were printing errors that apparently occurred during the printing process. Accordingly, it is believed that no fees are due in connection with the filing of this Request for Certificate of Correction. However, if it is determined that any fees are due, the Commissioner is hereby authorized to charge such fees to Deposit Account 500388 (Order No. NSC1P194D1).

Respectfully submitted,
BEYER WEAVER & THOMAS, LLP



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8. (original) The integrated circuit package, as recited in claim 2, wherein the lead posts have lengths which are substantially perpendicular to the conductive side of the first die.

9. (original) The integrated circuit package, as recited in claim 2, further comprising a second die with a conductive side and a side opposite the conductive side, wherein the side opposite the conductive side is connected to a side opposite the conductive side of the first die.

10. (original) The integrated circuit package, as recited in claim 9, further comprising wirebonding connected between the conductive side of the second die and at least one lead post of the plurality of lead posts.

11. (previously presented) An integrated circuit package comprising:

an array of lead posts that are equally spaced apart, each of the lead posts positioned on a an array of lead fingers, each of the lead fingers electrically isolated from one another, each of the lead posts further having an oversized contact pad on a bottom surface of the integrated circuit package, wherein each oversized contact pad has a diameter that is larger than a diameter of a respective lead post;

a first die having a conductive side that is electrically and mechanically connected to at least some of lead posts within the array of lead posts, wherein the conductive side of the first die faces the lead posts; and

an encapsulating material that encapsulates the first die and between the individual lead fingers of the array of lead fingers.

12. (original) An integrated circuit package as recited in claim 11 wherein the conductive side of each of the first dice is in direct contact with at least some of the lead posts.

13. (original) An integrated circuit package as recited in claim 11, further comprising:

a second die that is attached to the first die, wherein the second die has a conductive side and a side opposite the conductive side, wherein the side opposite the conductive side of each second die is connected to a side opposite the conductive side of the first die, wherein the second die has a plurality of conductive pads on the conductive side of the second die; and

interconnecting wires that connect the conductive pads of the second die to lead posts of the array of lead posts, wherein the encapsulating material also encapsulates the second die and each of the interconnecting wires.

14. (original) An integrated circuit package as recited in claim 11 wherein the encapsulating material has a top and a bottom surface and wherein each of the oversized contact pads are formed on the bottom surface of the encapsulating material.

15. (original) An integrated circuit package as recited in claim 11 wherein each of the oversized contact pads have a substantially square outline.

16. (previously presented)An apparatus, comprising,

a lead frame having a substantially continuous and planer first surface and a plurality of posts formed on the second surface;

a semiconductor die having an active surface, the active surface having a plurality of conductive pads in contact with the plurality of posts of the lead frame respectively;

an encapsulant material encapsulating the semiconductor die and the plurality of posts in contact with the plurality of conductive pads on the semiconductor die, the substantially continuous and planer second surface of the lead frame acting to prevent the encapsulant from forming on the second surface of the lead frame.

17. (previously presented)The apparatus of claim 16, wherein the encapsulant is formed between the plurality of posts.

18. (previously presented) The apparatus of claim 16, further comprising a conductive epoxy between the plurality of posts and the plurality of conductive pads respectively.

19. (previously presented) An apparatus, comprising:

a lead frame having a first surface and a substantially planar second surface,

a set of posts formed on the first surface of the lead frame, the plurality of post organized into a plurality of sub-sets of posts,

a plurality of semiconductor die, each of the plurality of die having conductive pads mounted onto the plurality of sub-sets of posts respectively; and

continuous encapsulant material encapsulating the lead frame including the plurality of semiconductor die and the plurality of sub-sets of posts, the substantially planer second surface of the lead frame acting to prevent the encapsulant from forming on the second surface of the lead frame.

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Approved for use through 6/30/99. OMB 0651-0033
Patent and Trademark Office; U.S. DEPARTMENT OF COMMERCE

(Also Form PT-1050)

UNITED STATES PATENT AND TRADEMARK OFFICE
CERTIFICATE OF CORRECTION

PATENT NO. : 6,975,038 B1 Page 1 of 1

DATED : December 13, 2005

INVENTOR(S) : Shahram Mostafazadeh

It is certified that error appears in the above-identified patent and that said Letters Patent are hereby corrected as shown below:

In the Claims:

In line 7 of claim 13 (column 9, line 2) change "fit die" to --first die--.

In line 13 of claim 19 (column 10, line 18) change "act to" to --acting to--.

MAILING ADDRESS OF SENDER:

PATENT NO. 6,975,038 B1

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